

**This Page Is Inserted by IFW Operations  
and is not a part of the Official Record**

## **BEST AVAILABLE IMAGES**

**Defective images within this document are accurate representations of the original documents submitted by the applicant.**

**Defects in the images may include (but are not limited to):**

- **BLACK BORDERS**
- **TEXT CUT OFF AT TOP, BOTTOM OR SIDES**
- **FADED TEXT**
- **ILLEGIBLE TEXT**
- **SKEWED/SLANTED IMAGES**
- **COLORED PHOTOS**
- **BLACK OR VERY BLACK AND WHITE DARK PHOTOS**
- **GRAY SCALE DOCUMENTS**

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/371,955	08/11/1999	SHANE P. LEIPHART	M4065.0196/P	9847

24998 7590 07/17/2002

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP  
2101 L STREET NW  
WASHINGTON, DC 20037-1526

EXAMINER

KANG, DONGHEE

ART UNIT	PAPER NUMBER
----------	--------------

2811

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/371,955

Applicant(s)

LEIPHART, SHANE P.

Examiner

Donghee Kang

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 02 April 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 26-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 26-40 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Acknowledgment*

1. Applicant's Amendment and Response to Paper No.13 has been entered and made of Record. Claims 26-40 are pending in this application.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **26-27** are rejected under 35 U.S.C. 102(b) as being anticipated by Fiordalice et al. (US 5,358,901).

Fiordalice teaches a semiconductor device, comprising (Fig.8):

a metallic layer (aluminum, 41) over a substrate (10); a dielectric layer (51) over said metallic layer (aluminum); a via hole (52, in Fig.5) extending through the dielectric layer to a surface of the metallic layer (41); a titanium aluminide layer (61) lining at least a bottom of the via hole; a conductive material (TiN, 72) on the titanium aluminide layer, said conductive material and said titanium aluminide layer being in contact at an interface; a conductive plug (73) material on the titanium nitride layer; and a metallic layer (74) on the dielectric layer and electrically connected to the plug material. See *also* Col.3, line 25 – Col.4, line 20.

Fiordalice does not explicitly teach the interface is substantially free from tensile stress between said titanium aluminide layer and said conductive material. However, this

feature is inherent because the conductive layer (72) is deposited after forming titanium aluminide layer. Therefore, claimed structure is taken to be in the least obvious over Fiordalice.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims **28-33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fiordalice et al. in view of Harada et al. (US 5,313,101) and further in view of Kanamori (US 5,281,850).

Regarding claims **28-32**, the teaching of Fiordalice was discussed above in section 3. See a statement of rejection of claim 26-27. Fiordalice teaches substantially the entire claimed structure except for a memory circuit region in a semiconductor substrate. However, Harada teaches in Fig.1 the memory circuit region (2) located on the substrate and is covered by an insulating layer (3). Thus, it would have been obvious in the art at the time the invention was made to have a DRAM or SRAM cell and interconnection layer in the ICs in order to make a memory device.

Neither Fiordalice nor Harada teaches an antireflective coating over a second dielectric layer. However, Kanamori teaches in Fig.1(f) the antireflecting coating layer (5) located at between aluminum layer and second dielectric layer. It is common to use a layer of material to suppress reflections from underlying surfaces during

photolithography exposure steps. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the antireflecting coating layer, since antireflecting coating layer suppresses reflections from underlying layers so that the photoresist is not exposed to the reflected light wave, which leads to variation in critical dimensions.

Regarding claim **33**, prior arts do not teach a substrate comprising a memory module. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have module system, since module system includes a plurality of components each storing or reading on binary bit at a time in the semiconductor memory device.

6. Claims **34-40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fiordalice in view of Harada and further in view of Clayton (US 4,656,605).

The teaching of Fiordalice as modified by Harada was discussed above in section 5.

Neither Fiordalice nor Harada teaches a memory module which include a semiconductor device. However, Clayton teaches the memory module comprising (Fig.2):

a substrate comprising a circuit board (31); a plurality of memory chips (10-18) mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprises a random access memory (RAM) fabricated on a semiconductor substrate; and an edge connector (20) along one edge of the substrate

which is wired to said memory circuit. Since Fiordalice and Clayton teach a DRAM, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Clayton with Fiordalice's device as modified by Harada in order to form module system that includes a plurality of components each storing or reading on binary bit at a time in the semiconductor memory device.

***Response to Argument***

7. Applicant's arguments with respect to claims 26-40 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Art Unit: 2811

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Donghee Kang, Ph.D.  
July 3, 2002

Steven Loke  
Primary Examiner  
*Steven Loke*